REMARKS

By this Amendment, claims 1, 8, and 12-14 are amended, and claims 29-39 are canceled. Accordingly, claims 1-16 are pending in this application. No new matter is added. Reconsideration of the application is respectfully requested.

Applicants thank Examiner Hogans for courtesies extended to Applicants' representatives during the September 2, 2004 personal interview. During the interview, possible amendments to claim 1 were discussed for clarification. Also, inconsistencies within the disclosure of the applied prior art were discussed. The substance of the interview is incorporated into the following, which constitutes Applicants' record of the interview.

A. The Office Action rejects claims 1, 4, and 5 under 35 U.S.C. §102(b) over U.S. Patent No. 5,498,554 to Mei. This rejection is respectfully traversed.

Claim 1 recites, *inter alia*, a high voltage well of a first circuit device is ion implanted in a first portion of a substrate using a partially removed first ion implantation protective layer to allow ion implantation at the first portion, and a first low voltage well of a second circuit device is ion implanted in a second portion of the substrate using the partially removed first ion implantation protective layer and a second ion implantation protective layer to allow ion implantation at the second portion.

The Office Action alleges that a nitride 220 corresponds to the first ion implantation protective layer. However, as discussed and agreed during the personal interview, the nitride 220 does not protect the substrate from the ion implantation as shown in Fig. 3B, in which an n-type dopant 40B is uniformly formed even under the nitride 220. Mei discloses only that the nitride 220 is used for oxide growth. See col. 4, lines 48-52. Therefore, Applicants respectfully submit that the nitride 220 cannot reasonably be considered to be a first ion implantation protective layer.

Mei discloses various photoresists in Figs. 3B-3F and 3I-3K. However, each of these photoresists is removed after the respective implantation. Thus, as discussed and agreed during the personal interview, a well of a second circuit device is not ion implanted in a portion of the substrate using a partially removed first ion implantation protective layer and a second ion implantation protective layer, as recited in claim 1. As such, Applicants respectfully submit that claim 1 is patentable over Mei.

Claims 4 and 5 are patentable at least in view of the patentability of claim 1, from which they depend, as well as for the additional features they recite. Accordingly, Applicants respectfully request withdrawal of the rejection based on Mei.

B. The Office Action rejects claims 1, 4, 5 and 8-13 under 35 U.S.C. §102(b) over U.S. Patent No. 6,686,233 to Soderbarg et al. (Soderbarg). This rejection is respectfully traversed.

As discussed and agreed during the interview, Soderbarg does not teach or suggest that a well of a circuit device is ion implanted in a portion of the substrate using a partially removed first ion implantation protective layer and a second ion implantation protective layer to allow ion implantation at the second portion. As such, Applicants respectfully submit that claim 1 is patentable over Soderbarg.

Claims 4, 5 and 8-13 are patentable at least in view of the patentability of claim 1, from which they depend, as well as for the additional features they recite. Accordingly, Applicants respectfully request withdrawal of the rejection based on Soderbarg.

C. The Office Action rejects claim 2 under 35 U.S.C. §103(a) over Mei in view of U.S. Patent No. 5,519,247 to Arbus et al. (Arbus). This rejection is respectfully traversed.

Arbus does not overcome the deficiencies of Mei with respect to claim 1. Therefore, claim 2 is patentable at least in view of the patentability of claim 1, from which it depends, as

well as for the additional features it recites. Accordingly, withdrawal of this rejection is respectfully requested.

D. The Office Action rejects claim 3 under 35 U.S.C. §103(a) over Mei in view of U.S. Patent No. 6,444,487 to Boggs et al. (Boggs). This rejection is respectfully traversed.

Boggs does not overcome the deficiencies of Mei with respect to claim 1. Therefore, claim 3 is patentable at least in view of the patentability of claim 1, from which it depends, as well as for the additional features it recites. Accordingly, withdrawal of this rejection is respectfully requested.

E. The Office Action rejects claims 6 and 7 under 35 U.S.C. §103(a) over Mei in view of U.S. Patent No. 6,130,458 to Takagi et al. (Takagi). This rejection is respectfully traversed.

Takagi does not overcome the deficiencies of Mei with respect to claim 1. Therefore, claims 6 and 7 are patentable at least in view of the patentability of claim 1, from which they depend, as well as for the additional features they recite. Accordingly, withdrawal of this rejection is respectfully requested.

F. The Office Action rejects claim 1 under 35 U.S.C. §103(a) over U.S. Patent No. 6,258,701 to Depetro et al. (Depetro) in view of Mei. This rejection is respectfully traversed.

Claim 1 recites, *inter alia*, a high voltage well of a first circuit device is ion implanted in a first portion of a substrate using a partially removed first ion implantation protective layer to allow ion implantation at the first portion, and a first low voltage well of a second circuit device is ion implanted in a second portion of the substrate using the partially removed first ion implantation protective layer and a second ion implantation protective layer to allow ion implantation at the second portion.

As discussed and agreed during the personal interview, Depetro has inconsistencies in its disclosure. For example, col. 3, lines 46-57 describes that a portion of a silicon oxide layer 12 is removed to create a window 14 with vertical walls 16 for forming an oxide region 12' at a low voltage active area. Col. 3, lines 58-60 describes that a portion of a second resist mask 17 and a portion the oxide layer 12 are removed to create a window 18 with inclined walls 23 for forming an oxide region 12" at a high voltage active area. However, col. 4, lines 11-16 describes that "a portion of a wafer delimited by the oxide regions 12" with the vertical walls 16 is suitable for forming high voltage components, whereas the portion of the wafer delimited by the oxide region 12" with their inclined walls 23 is suitable for forming low voltage components" (emphasis added). Col. 5, lines 10-32 has similar inconsistencies.

However, in the Background Of The Invention section, Depetro recognizes that high voltage devices require insulating structures with degrading walls to prevent early breakdown, while low voltages do not present this problem. Depetro then describes, in the Summary Of The Invention section, its object to provide a process for forming insulating structure that helps integration of high voltage components using inclined walls, as well as low voltages components using vertical walls.

Reading Depetro as a whole, Applicants respectfully submit that any apparent teaching that a portion of a wafer delimited by the oxide regions 12" with the vertical walls 16 is suitable for forming high voltage components, whereas the portion of the wafer delimited by the oxide region 12" with their inclined walls 23 is suitable for forming low voltage components in Depetro is an error. For proper consisting throughout the disclosure of Depetro, this passage should have read "a portion of a wafer delimited by the oxide regions 12" with the vertical walls 16 is suitable for forming low voltage components, whereas the portion of the wafer delimited by the oxide region 12" with their inclined walls 23 is suitable for forming high voltage components."

Furthermore, as discussed and agreed during the personal interview, Depetro discloses a process to form low voltage active areas prior to high voltage active areas. In other words, Depetro discloses only a process for forming the vertical walls prior to forming the inclined walls. Applicants respectfully submit that one of ordinary skill in the art would not have been motivated to modify the process taught by Depetro in order to achieve the claimed feature of forming a high voltage well first and then forming a low voltage well.

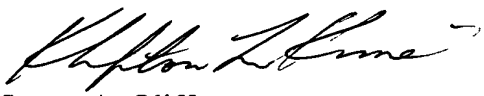
As such, Applicants respectfully submit that claim 1 is patentable over Depetro and Mei. Thus, withdrawal of this rejection is respectfully requested.

IV. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-16 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,



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